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Functional SOFC Interfaces Created by Aerosol-Spray Deposition

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Abstract

In the development of solid-oxide fuel cells, coating technologies are essential to successful commercialization. Electrode coating technologies allow the cost-effective deposition of barrier layer, anode and cathodes on cell components at high volumes and high precision. Specialized oxide protective layers are also important to making low-cost steel interconnectors corrosion-resistant at SOFC operating while maintaining low contact resistance and minimizing Cr volatilization. Finally, catalytic and corrosion resistant coatings for common steel alloys find application in gas delivery and fuel reforming components of the balance-of-plant.

Nexceris has developed a suite of contact paste, insulating layer coatings and catalytic materials for SOFC stacks and balance of plant, all designed with the end-user needs in mind. Leveraging aerosol spray deposition approaches that have been scaled to commercial requirements, Nexceris can interleave these coatings to create uniquely functional interconnects, cells and reformer components.

A novel aerosol-spray based coating approach to enhance electrolyte/electrode barrier layer interfaces by enabling low temperature processing that prevent detrimental cathode/electrolyte interactions will be discussed. Electrochemical impedance spectroscopy has been used to understand how the deposition conditions and the barrier layer formulation can be tailored to minimize the electrolyte/electrode interface resistance. Single-cell and stack-level testing will demonstrate the applicability of this approach to improve performance of both electrolyte and anode-supported cell designs. Furthermore, it will be shown how a similar approach can be utilized to create chemically inert surfaces for glass bonding that are thermal expansion matched to SOFC cells and interconnects.

Introduction

Solid oxide fuel cell (SOFC) systems are emerging as a highly-desirable premium power technology. Commercial customers with mission-critical power requirements are recognizing SOFCs can uniquely serve as baseload generators in mobile or micro-grid power generation scenarios, offering quiet, efficient power generation on a range of fuels. The financial reward provided by these premium applications pales in comparison to that offered by commercial residential or transportation power systems. Today's state-of-the-art SOFC's offer great promise, but not at commercially viable costs. To move these technologies beyond niche applications and proof of-concept demonstrations, the cost must be reduced. An important approach to reduce SOFC system cost is to increase the power generated by the cell itself. By reducing the intrinsic SOFC cell resistance, resulting stacks can be smaller and less expensive.

The interface between the SOFC cathode and the electrolyte layer is the highest resistance interface on the cell and has long been targeted as the most promising location to enhance cell performance. Ceria barrier layers are a critical feature of high performance SOFCs [1,2]. The vast majority of SOFCs have cathode materials that contain strontium as a dopant to enhance oxygen diffusion [3]. Common examples include LSM $(La,Sr)MnO_3$ and LSCF $(La,Sr)(Co,Fe)O_3$. While strontium enhances cathode performance, it is prone to adverse reactions with zirconia-based electrolytes, resulting in the formation of a resistive strontium zirconate $(SrZrO_3)$ interfacial phase [4,5]. By depositing a thin samarium-doped ceria (SDC) layer at the cathode-electrolyte interface, $SrZrO_3$ formation can be avoided, while simultaneously enhancing oxygen transfer from the cathode to the electrolyte layer [6]. Together, these features allow barrier layers of SDC, when applied to YSZ electrolytes to enhance the performance of resulting SOFCs. As a result, rare-earth doped ceria based barrier layers are commonly implemented in SOFC manufacture. However, achieving the full benefit of SDC barrier layers is challenging.

The limitations of conventional SOFC manufacturing approaches for creating an effective barrier layer are well documented. To allow integration with other fabrication steps, SDC layers typically are deposited by screen-printing, painting or spray deposition of ceramic powder slurries [7], and then densified at high temperatures (T ≥ 1200 °C). These deposition approaches result in relatively porous barrier layers that fail to completely prevent $SrZrO_3$ formation during cathode deposition. These processes also result in reaction between barrier layer and electrolyte to form electrically resistive zirconium doped ceria (ZDC). For example, as shown by Endler-Schuck et al. [8], the theoretical contribution of a 7-micron thick doped-ceria electrolyte to overall cell resistance at 700ºC should be ~0.02 Ω-cm^2, but assuming 2 microns of ZDC formation, it becomes 0.10 Ω-cm^2, which matches well with measured values for screen-printed samples fired at 1300ºC. Given that the electrolyte resistance of the cell is calculated to be only 0.005 Ω-cm^2, this is a major issue.

Several techniques have shown the gap between actual sintered ceria barrier layers and the theoretical goal can be minimized through growth of dense ceria coatings at low temperatures. For example, in the previously mentioned study [8], experimental results confirming the proposed theoretical limits were obtained using Metal Organic Deposition processing. By using this approach, the group was able to reduce processing temperatures to 400ºC and produce cells with half the ASR of screen printed cells, but still experienced some degree of interaction between the cathode and zirconia layers, due to diffusion through

the relatively thin (50-100 nm) Gd-doped ceria layers. Further, multiple coating steps were required to achieve these thicknesses, economically challenging it and other spin coating or pad printing approaches to metal-organic derived layers.

As another example, researchers at Pacific Northwest National Laboratory (PNNL) have demonstrated that dense SDC barrier layers deposited by Pulse layer deposition (PLD) successfully prevent $SrZrO3$ formation and resulting in lower ohmic contribution to cell resistance, dropping from 0.22 to 0.13 Ω-cm^2 [9]. Unfortunately, as acknowledged in the study, PLD is an expensive deposition technique, which is difficult to scale to high-volume production.

In addition to these studies, wet slurry deposition approaches have been considered for barrier layers, seeking to use high surface area powders and increasing green density. These approaches often rely upon the addition of dopants and/or high surface area powder synthesis to enhance sinterability of the deposited layer [9,10].

1. Scientific Approach

This paper reviews the development of a new cathode/electrolyte interfacial layer that forms a dense, protective barrier at lower annealing temperatures than traditional processes. An aerosol-spray deposition (ASD) approach has been developed that provides excellent control of layer thickness and uniformity. The combination of higher sinterability powder, deposited through a controlled deposition approach produces a thin, dense SDC barrier layer which significantly reduces the resistance of the cathode/electrolyte interface.

2. Experiments/Calculations/Simulations

A wide-range of both traditional (transition metal oxides) and more novel sintering aids have been evaluated to identify highly sinterable SDC powder formulations. A SDC20 powder (***fuelcell**materials.com*) with surface area of 11.7 m^2/g and particle size (d$_{50}$) of 0.21 µm was used, and the various dopants screened at different loadings and integration approaches through sintered density measurements and dilatometry.

Promising doped SDC20 powders, that demonstrated improved sinterability were down-selected for further evaluation. The powders were made into solvent-based spray suspensions and applied as thin barrier-layer coatings to scandia-stabilized zirconia (ScSZ) button-cell electrolytes (20 mm diameter) through aerosol-spray deposition (ASD) using a PRISM300 ultrasonic spray system (*Ultrasonics Inc.*). Through ASD, micron-level control of coating thickness is achievable. Nominal coating thicknesses of 3-5 µm were targeted.

The effect of barrier-layer annealing temperature and cathode processing on the electrical behavior of the ScSZ electrolyte/cathode interface was investigated through half-cell electrochemical impedance spectroscopy (EIS) using a three-electrode, asymmetric button-cell configuration. A LSCF cathode was applied to the barrier layer and used as the working electrode, with a platinum counter, and annulus reference electrodes to enable de-convolution of the electrical behavior across the electrolyte/cathode interface, and an assessment of how changes to the barrier layer microstructure affects electrical resistance.

The microstructure of the barrier-layer and electrolyte/cathode interface was evaluated by cross-sectional scanning electron microscopy (SEM) and compositional energy dispersive

spectroscopy (EDS), using a JEOL JSM840-A Scanning Electron Microscope in conjunction with an EDS system manufactured by PGT/Bruker.

Based on the results from the EIS and microstructural analysis a barrier-layer formulation and process was down-selected for large-area single-cell testing using Nexceris' 28 cm^2 test-platform. Both electrolyte and anode-supported cells have been built, cured and reduced in a furnace following Nexceris' standard stack processing protocols. Cell-performance was determined from V-I polarization curves in diluted hydrogen fuel (50/50 H_2/N_2) at different furnace temperatures.

3. Results

Figure 1 shows representative real impedance Bode plot at 700°C (Figure 1a), and corresponding Arrhenius plot of polarization resistance (Figure 1b) for half-cells with no barrier-layer, traditional screen-printed barrier-layer, and Nexceris' new ASD barrier layer. It is clear that incorporating a ceria barrier layer at the electrolyte-cathode interface is beneficial, significantly reducing the interfacial resistance. Furthermore, Nexceris' ASD barrier-layer reduces the electrolyte-cathode resistances more than an order of magnitude compared to a traditional screen-printed barrier-layer.
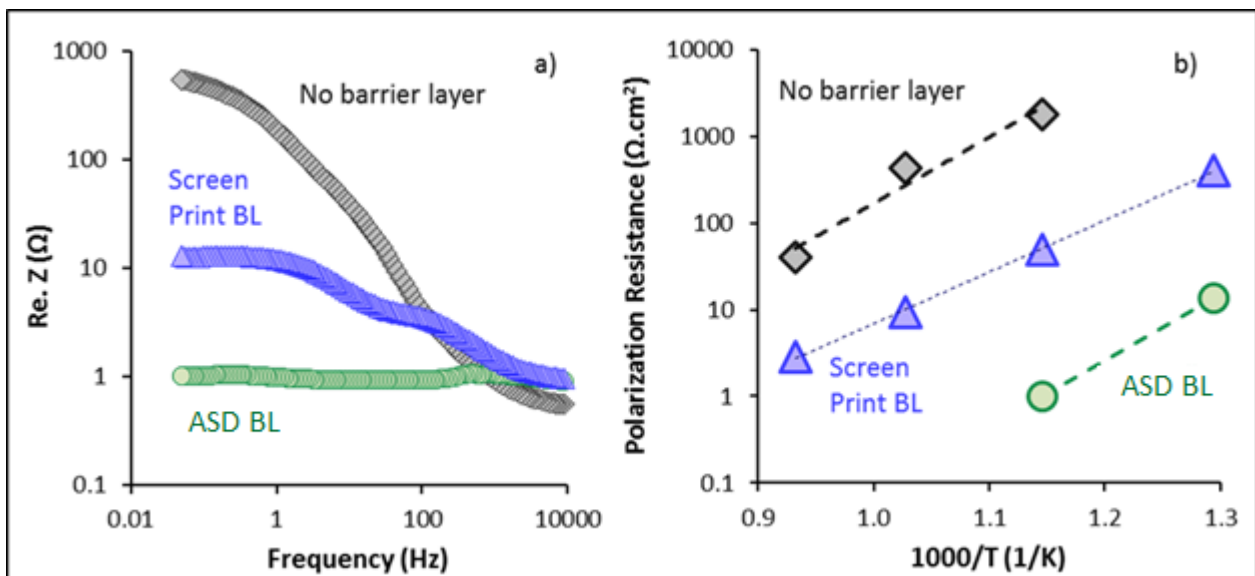

Figure 1. Representative Real Impedance Bode Plot at 700 °C (a), and corresponding Arrhenius plot of polarization resistance (b), for ESC half-cells with no barrier layer, screen-printed SDC, and ASD SDC barrier layer.

Figure 2 shows the single-cell V-I polarization curves for Nexceris' electrolyte-supported *NextCell*™ (Figure 2a), and anode-supported cells (Figure 2b) with traditional SDC barrier-layer and ASD based barrier-layers.
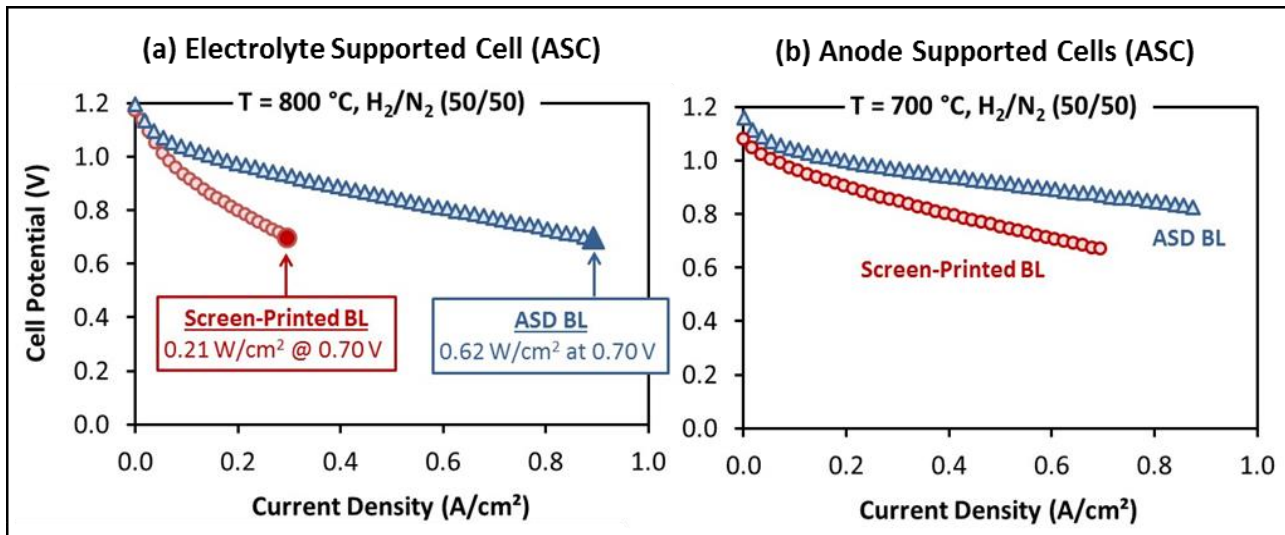
Figure 2. Single-cell performance of Nexceris' electrolyte-supported *NextCell*TM (a), and anode-supported cell (b), with screen printed, and ASD based SDC barrier layers.

Post-test microstructural analysis was used understand the reduction in cell resistance and improvement in cell performance demonstrated for Nexceris' ASD barrier layer. Figure 3 shows cross-section SEM images with superimposed EDS elemental mapping of the electrolyte-cathode interface of electrolyte-supported cells with screen-printed (Figure 3a), and ASD barrier-layer (Figure 3b).
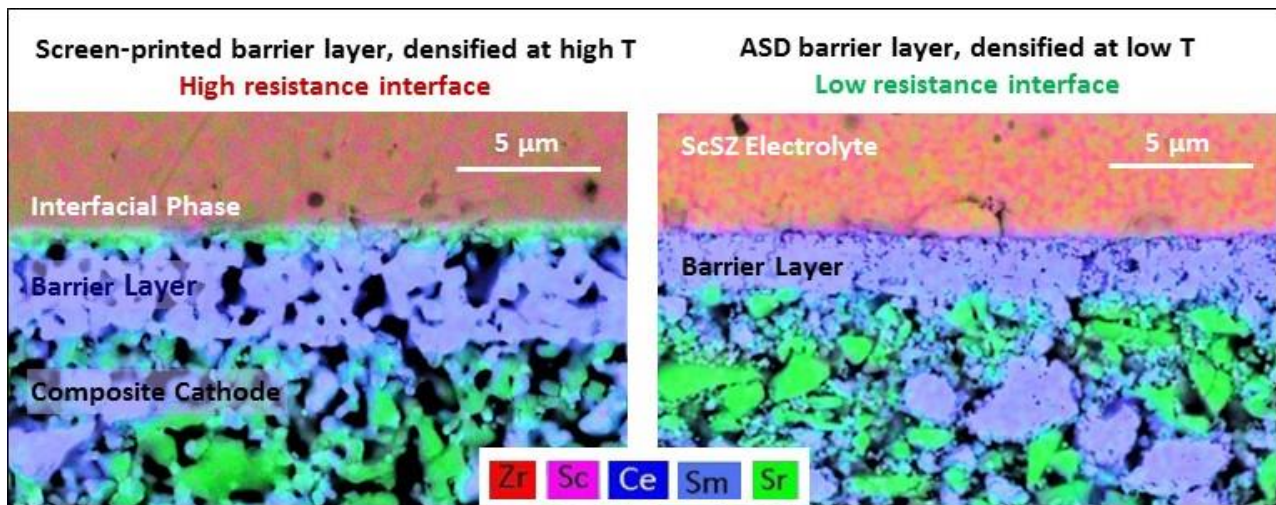
Figure 3. SEM microstructures of the cathode/electrolyte interface with standard barrier layer fired at 1300 °C (a), and ASD barrier layer (b), and after single-cell testing.

The screen-printed barrier-layer is porous, and has a very obvious interfacial reaction with the electrolyte, while the ASD barrier-layer cell has a dense SDC barrier layer and no evidence of an interfacial phase. The elimination of these resistive interfacial phases enables Nexceris' barrier-layer technology to reduce cell costs ($/kW) by increasing cell performance and lowering manufacturing costs (more easily scalable and lower cost ASD process).

Acknowledgments

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